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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/809,888 | 03/26/2004 | Akimitsu Ikeda | 107337-00057 | 7772 |

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ARENT FOX PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

| EXAMINER | |
|---|---|
| KERVEROS, JAMES C | |
| ART UNIT | PAPER NUMBER |
| 2138 | |

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/809,888 | IKEDA ET AL. | |
| | Examiner | Art Unit | |
| | JAMES C. KERVEROS | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7 and 8* is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/3/06, 9/11/05* 3/24
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This is a Non-Final Action in response to the instant U.S. Application filed 03/26/2004. Claims 1-8 are pending and presently under examination.

### *Priority*

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), for JP Application No. 2003-297210, filed 08/21/2003. The certified copy has been filed in parent instant Application No. 10/809,888, filed on 03/26/2004.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Lindsay et al. (US PATENT NO: 6,634,005) filed: May 1, 2000.

Regarding Claim 1, Lindsay discloses a semiconductor device test circuit (boundary scan system 300, Figure 6) in compliance with the IEEE Standard 1149.1, Standard Test Access Port and Boundary-Scan Architecture, including boundary scan

cells (302, 304, 306, 308) connected through the boundary scan ring 301, for testing a functional macro circuit (on-chip logic 102) in the integrated circuit 100 shown in Figure 1, the test circuit comprising:

A plurality of first flip-flop circuits (flip-flops 186A-D) connected in series in the boundary scan cells, so that serial test pattern data (test data, TDI) supplied serially to the input of boundary scan ring 301 through data inputs (194A-D) of multiplexers (182A-D). The serial data are latched at first flip-flop circuits (flip-flops 186A-D) in synchronization with a first clock signal (clock DR signal 258), which synchronously clocks flip-flops (186A-D).

A plurality of second flip-flop circuits (flip-flops 188A-D) for outputting the test pattern data latched by the plurality of first flip-flop circuits (flip-flops 186A-D) into the functional macro circuit (on-chip logic 102) in synchronization with a second clock signal (update DR signal 260). It is noted that the boundary scan cells (302, 304, 306, 308) of Figure 6 are configured as input scan cells corresponding to boundary scan cells (120, 122, 124, 126) of Figure 1, for inputting the test pattern data into the functional macro circuit (on-chip logic 102).

Regarding Claim 2, Lindsay discloses the plurality of first flip-flop circuits (flip-flops 186A-D) and the plurality of second flip-flop circuits (flip-flops 188A-D) are delayed flip-flop circuits, since they are driven by two different clocks (clock DR signal 258) and (update DR signal 260), which are delayed with respect to each other.

Regarding Claims 3, Lindsay discloses selector circuits (multiplexers 184A-D) for selecting the test pattern data outputted from each of the plurality of second flip-flop

circuits (flip-flops 188A-D) or a signal from a user logic and outputting the selected test pattern data or the selected signal to the functional macro circuit (on-chip logic 102) in accordance with a control signal (select input 196A-D). Figure 5 illustrates the mode signal to be input into a specific boundary scan cell at the select input of a multiplexer, such as select input 196 of multiplexer 184 of boundary scan cell 180 shown in Figure 3. If a logic 1 is applied to select input 196, output signal 224 corresponds to test data which has been shifted through the boundary scan chain to flip-flop 186 and then clocked to the output of flip-flop 188. Conversely, if the logic signal entering select input 196 of multiplexer 184 is logic 0, output signal 224 corresponds to data signal 212.

Regarding Claims 4-6, Lindsay discloses (boundary scan system 300, Figure 6) including boundary scan cells (302, 304, 306, 308) connected in series through the boundary scan ring 301 configured to output data from the functional macro circuit (on-chip logic 102), which includes a selector circuit (multiplexer 182A) and a third flip-flop circuit (186A), wherein a signal (302) outputted from the functional macro circuit (on-chip logic 102), and the test pattern data outputted from the first flip-flop circuit at a last stage (From Last Cell, 194A) are inputted to the selector circuit (multiplexer 182A) at a first stage, while a signal outputted from the functional macro circuit (304) and a signal outputted from the third flip-flop circuit (186A) at a preceding stage are inputted to the selector circuit (182B) at each of subsequent stages, further wherein the third flip-flop circuit (186A), latches a signal selected by the selector circuit (182A) in synchronization with the first clock signal (Clock DR), Figure 6, and wherein the third flip-flop circuit (186A) is a delayed flip-flop circuit by (Clock DR). And wherein the third flip-flop circuit

(186D) included in the circuit at a last stage (boundary scan cell 308) serially outputs the test pattern data (To Next Cell) or the signal (308) outputted from the functional macro circuit (on-chip logic 102).

***Allowable Subject Matter***

Claims 7 and 8 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention recited in the independent claim 7, including among other limitations, "a plurality of third flip-flop circuits, the number of the plurality of third flip-flop circuits depending on the number of the plurality of semiconductor device test circuits, connected in series for outputting a control signal for specifying one of the plurality of semiconductor device test circuits in synchronization with a third clock signal".

Claim 8 depends from claim 7 and therefore is allowable.

Consequently, claims c7 and 8 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

3/29/2006